photolithographic masking layer 24 that is disposed atop a wafer 120, and *source/drain vertical trenches* 172 are etched in the openings 170 down to a buried top gate insulator layer 160'. Then, a doped layer 174 is formed on the sidewalls of the *source/drain vertical trenches* 172, and the *source/drain vertical trenches* 172 are further etched down to a bottom gate insulator layer 160". Gate sidewall spacers 176 are then formed on the sidewalls of the *source/drain vertical trenches* 172, and source/drain regions 180 are formed at the bottom of the trenches. The part of the bottom gate insulator 160" at the bottom of the trenches is removed, and the trench is filled with a conductive material 189. (See Figs. 3c-3g; and col. 11, line 36 to col. 14, line 44.) Clearly, a vertical trench structure that electrically contacts a source/drain region is a *source/drain contact*, rather an *isolation trench*. (See col. 11, lines 40-45; col. 13, lines 56-58; and col. 14, lines 50-51.)

Moreover, though the Examiner acknowledges that the Kenney patent fails to disclose a trench enclosing an area of the semiconductor body that contains a semiconductor structure, he nonetheless contends that it would still have been obvious to modify the device of Kenney in such a manner as shown by Kagaya. However, Kenney describes *source/drain vertical trenches* rather than *isolation trenches*, as noted above, and thus there is no incentive from Kagaya to modify *source/drain trenches* to enclose an area of a semiconductor body in the manner of an isolation trench. Not only would such modification of the source/drain vertical trenches not be advantageous, it would needlessly complicate the structure of Kenney's device and make Kenney's device non-functional.

It follows that neither Kenney nor Kagaya suggests:

> the semiconductor body defining an isolation trench having a bottom and sidewalls and having an upper portion and a lower portion, said isolation trench enclosing an area of the semiconductor body which contains a semiconductor structure which is to be electrically isolated from other semiconductor structures that are also contained within the semiconductor body but which are not located within the enclosed area

as called for in claim 1.

Further, though Kenney describes an isolation trench, the isolation trench clearly differs from the structure defined in claim 1. Namely, Kenney describes an isolation trench 192 that is filled with an insulator material 194 to passivate the exposed sidewalls of the trench 192, as shown in Figs. 3b and 3h. (See also col. 12, lines 51-65.)

The Kagaya patent does not remedy the deficiencies of Kenney. The patent describes compound semiconductor integrated circuits in which an element separating trench 9 is opened down to a semi-insulating substrate 1 and encloses the periphery of a FET. The trench may be filled with an insulator. (See Figs. 1, 2, 3, 6E, 8, 19, 25, 28, and 30; col. 3, lines 8-10; and col. 9, lines 3-13.)

Thus, neither Kenney nor Kagaya suggests an *isolation trench* having a lower portion filled with electrically conductive material, nor does Kenney or Kagaya suggest electrically conductive material that is separated from the sidewalls of an *isolation trench*.

Neither reference suggests:

> the lower portion of the isolation trench being at least partly filled with an electrically conductive material that has sidewall portions which are at least partly separate from the sidewalls of the lower portion of the isolation trench by a first electrical insulator, said electrically conductive material having a lower portion that is in electrical contact with the semiconductor body at the bottom of said isolation trench

as recited in claim 1.

Kenney also describes that the wafer may then be further processed to form two contacts in a single trench. The first conductive layer is etched back below the trench opening, and a layer of insulator 210 is then deposited atop the first conductive layer and one the sidewalls of the trench. A portion of the now exposed part of the trench is then widened, and the remainder of the trench is then filled with a second *conductor* 214. Kenney does not suggest filling an upper portion of the trench with an *electrical isolator*. (See Figs. 5a-5d; col. 14, lines 50-51; and col. 14, line 58 to col. 15, line 5.)

Moreover, Kagaya describes filling the trench with a *single insulator*, and does not suggest a *second* insulator. Neither Kenney nor Kagaya suggests:

> the upper portion of the isolation trench being filled with a second electrical insulator.

as defined in claim 1.

It follows that neither Kenney, Kagaya, nor their combination suggests or contemplates the method called for in claim 1 and that claim 1 is patentably distinct and unobvious over the references.

Claim 2 depends from claim 1 and further defines and limits the invention set out in the independent claim as well as calls for additional limitations. It follows that claim 2 likewise defines a combination that is patentably distinguishable over the references.

Accordingly, the withdrawal of the rejection of claims 1-2 under 35 U.S.C. § 103 is respectfully requested.

As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that the Examiner telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which the Examiner might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

By _____

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